PATENT

Atty Docket No.: 10013828-1
App. Ser. No.: 10/067,317

REMARKS

Favorable reconsideration of this application is respectfully requested in view of the following remarks. Claims 1, 4-9, and 11-16, and 18-23 are pending in the present application of which claims 1, 11 and 16 are independent. Claims 1, 11 and 16 have been amended. Claims 2, 3, 10 and 17 have been cancelled. Claims 21, 22 and 23 have been added. No new matter has been added by way of the claim amendments and additions, and entry thereof is therefore respectfully requested.

Claim 1 stands rejected under 35 U.S.C. § 102(b) as allegedly being anticipated by Grzyb et al. (U.S. Patent No. 5,656,834) ("Grzyb et al."). Claims 16 and 20 stand rejected under 35 U.S.C. § 102(e) as allegedly being anticipated by Appel (U.S. Patent No. 6,653,681) ("Appel"). Claims 2-4, 6-13 and 15 stand rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over Grzyb et al. in view of Appel. Claims 17-19 stand rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over Appel in view of Grzyb et al. Claims 5 and 14 stand rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over Grzyb et al. in view of Appel, and further in view of Daubenspeck et al. (U.S. Patent No. 6,496,053) ("Daubenspeck et al."). The rejections are respectfully traversed for at least the following reasons.

Election/Restriction

The Applicants acknowledge the withdrawal of the restriction requirement mailed on December 3, 2004.

Drawings

At the outset, the indication that the drawings filed on February 7, 2002 have been accepted is noted with appreciation.

Claim Rejection under 35 U.S.C. 102

The test for determining if a reference anticipates a claim, for purposes of a rejection under 35 U.S.C. § 102, is whether the reference discloses all the elements of the claimed combination, or the mechanical equivalents thereof functioning in substantially the same way to produce substantially the same results. As noted by the Court of Appeals for the Federal Circuit in *Lindemann Maschinenfabrick GmbH v. American Hoist and Derrick Co.*, 221 USPQ 481, 485 (Fed. Cir. 1984), in evaluating the sufficiency of an anticipation rejection under 35 U.S.C. § 102, the Court stated:

> Anticipation requires the presence in a single prior art reference disclosure of each and every element of the claimed invention, arranged as in the claim.

Therefore, if the cited reference does not disclose each and every element of the claimed invention, then the cited reference fails to anticipate the claimed invention and, thus, the claimed invention is distinguishable over the cited reference.

Rejection of Claim 1 under 35 USC 102(b)

The Office Action sets forth a rejection of claim 1 under 35 USC 102(b) as allegedly being anticipated by Grzyb et al. (U.S. Patent No. 5,656,834) ("Grzyb et al."). This rejection is respectfully traversed.

Independent claim 1 recites a method of forming an integrated circuit comprising "forming an inter-digitated capacitance structure in an area above the circuit function block, wherein forming the inter-digitated capacitance structure comprises forming a plurality of inter-digitated metal fingers extending outward from at least one inter-digitated metal" and "forming a plurality of de-coupling capacitances between the inter-digitated capacitance structure, the top metal layer and bottom metal layer, and the dielectric material." Amended independent claim 1 incorporates the features of cancelled claims 2, 3 and 10.

Grzyb et al. discloses integrated circuits (ICs) provided with capacitors to reduce radio frequency interference (RFI). (Column 2, lines 1-10) According to Grzyb et al., integrated circuits running at high frequencies are a potential source of RFI (Col. 1, line 60). .

Grzyb et al. fails to teach "forming an inter-digitated capacitance structure in an area above the circuit function block" as recited in independent claim 1. Instead, Grzyb et al. discloses an IC fabricated in a p-type silicon substrate 26 which is provided with n-wells 27 (Column 3, lines 63-67). Grzyb et al. further discloses that an n-well 27 is used to house a decoupling capacitor 20 (Column 4, lines 1-3).

The Office Action cites column 3, line 65 through column 4, line 3 of Grzyb et al. stating

> Grzyb et al. disclose a method of forming an integrated circuit where a circuit function block is formed on an IC chip; and forming a decoupling capacitor (20) in an area above the circuit function block" (Office Action, page 2)

However, the cited passage of Grzyb et al. fails to teach "forming an inter-digitated capacitance structure in an area above the circuit function block" as recited in independent claim 1. Nowhere does Grzyb et al. disclose an inter-digitated capacitance structure. Moreover, Grzyb et al. fails to teach that the capacitor 20 is an inter-digitated capacitance structure.

In addition, Grzyb et al. fails to teach "forming a plurality of de-coupling capacitances between the inter-digitated capacitance structure, the top metal layer and bottom metal layer, and the dielectric material" as recited in claim 1. Specifically, the capacitor 20 of Grzyb et al. does not provide "a plurality of de-coupling capacitances." Instead, the capacitor 20 provides a single capacitor having an oxide layer as a dielectric (Column 4, lines 1-5). Furthermore, the capacitor 20 is not an inter-digitated capacitance structure. Grzyb et al. thus fails to teach forming a plurality of de-coupling capacitances between an inter-digitated capacitance structure, a top metal layer, a bottom metal layer, and a dielectric material. For at least these reasons, Grzyb et al. fails to teach each and every feature of claim 1. Claim 1 is thus allowable over Grzyb et al., and withdrawal of the rejection is respectfully requested.

Rejection of Claims 16 and 20 under 35 USC 102(e)

The Office Action sets forth a rejection of claims 16 and 20 under 35 USC 102(e) as allegedly being anticipated by Appel et al. (U.S. Patent No. 6,653,681) ("Appel et al."). This rejection is respectfully traversed.

Independent claim 16 recites an integrated circuit comprising "a circuit function block having a predetermined circuit layout" and "an inter-digitated capacitance structure comprising at least one metal plate and a plurality of inter-digitated metal fingers on top of the circuit function block, wherein a plurality of de-coupling capacitances are formed between the inter-digitated capacitance structure, a first metal layer, and a second metal layer." Amended independent claim 16 incorporates the features of cancelled claim 17.

Appel discloses a metal-insulator-metal (MIM) capacitor. (Abstract; Column 1, lines 45-50) According to Appel, the MIM capacitor includes metallized lines (Column 2, line 22).

Appel fails to teach "a circuit function block having a predetermined circuit layout," "an inter-digitated capacitance structure...on top of the circuit function block" and "a plurality of de-coupling capacitances" as recited in independent claim 16. Appel discloses a MIM capacitor having five metal layers MET1-MET5 (Figure 2; Column 2, lines 30-35), but fails to teach an inter-digitated capacitance structure on top of a circuit function block, wherein the circuit function block has a predetermined circuit layout.

The rejection cites Column 1, lines 31-37 of Appel and paraphrases this passage stating

> Appel discloses an integrated circuit where a circuit function block has a predetermined circuit layout; and an inter-digitated capacitance structure comprising at least one metal plate and a plurality of inter-digitated metal fingers on top of the circuit function block. (Office Action, page 3)

This rejection appears to be unsupported by the disclosure of Appel. Specifically, Appel fails to teach any type of circuit function block, and also fails to teach that the MIM capacitor having the five metal layers MET1-MET5 is "on top of the circuit function block," further wherein the circuit function block has "a predetermined circuit layout" as claimed. In addition, Appel fails to teach any reference of the MIM capacitor in relation to a circuit function block having a predetermined circuit layout.

In addition, Appel fails to teach "forming a plurality of de-coupling capacitances" as recited in independent claim 16. Instead, Appel discloses a MIM capacitor having five metal layers MET1-MET5 (Figure 2; Column 2, lines 30-35), but Appel fails to teach that the MIM capacitor provides a plurality of de-coupling capacitances.

For at least these reasons, Appel fails to teach each and every feature of independent claim 16. Because dependent claim 20 incorporates all the features of independent claim 16, Appel fails to anticipate the invention claimed in claim 20 for at least the reasons given

above. Claims 16 and 20 are thus allowable over Appel, and withdrawal of the rejection is respectfully requested.

Claim Rejection Under 35 U.S.C. §103

The test for determining if a claim is rendered obvious by one or more references for purposes of a rejection under 35 U.S.C. § 103 is set forth in MPEP § 706.02(j):

> To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art and not based on applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).

Therefore, if the above-identified criteria are not met, then the cited reference(s) fails to render obvious the claimed invention and, thus, the claimed invention is distinguishable over the cited reference(s).

Rejection of Claims 2-4, 6-13 and 15 under 35 U.S.C. § 103(a)

The Office Action sets forth a rejection of claims 2-4, 6-13 and 15 under 35 U.S.C. § 103(a) as allegedly being unpatentable over Grzyb et al. in view of Appel. This rejection is respectfully traversed for at least the following reasons.

Claims 2, 3 and 10 have been cancelled and the features of claims 2, 3 and 10 have been incorporated into amended independent claim 1. The features of claims 2, 3 and 10 are neither taught nor suggested by Grzyb et al. or Appel, for at least the reasons set forth below.

Grzyb et al. fails to teach or suggest that the capacitor 20 provides a plurality of de-coupling capacitances. Instead, the capacitor 20 provides a single capacitor having an oxide

layer as a dielectric (Column 4, lines 1-5). Furthermore, the capacitor 20 is not an inter-digitated capacitance structure.

In addition, Appel fails to remedy the deficiencies of Grzyb et al. Appel discloses a MIM capacitor, but Appel fails to teach or suggest "forming a circuit function block on an IC chip" as recited in independent claim 1. Nowhere does Appel teach or suggest a circuit function block on an IC chip. Neither does Appel teach or suggest "forming a plurality of de-coupling capacitances" as recited in independent claim 1. Instead, Appel discloses a MIM capacitor having five metal layers MET1-MET5 (Figure 2; Column 2, lines 30-35), but Appel fails to teach or suggest that the MIM capacitor provides a plurality of de-coupling capacitances. Thus, neither Grzyb et al. nor Appel teach or suggest all the features of independent claim 1 and claims 4 and 6-9, which incorporate all the features of claim 1.

Claims 12-13 and 15 incorporate all the features of independent claim 11.

Independent claim 11 recites a method comprising, *inter alia*, "forming a circuit function block on an IC chip" and "wherein forming the inter-digitated capacitance structure further comprises forming a plurality of de-coupling capacitances between the inter-digitated capacitance structure, the first metal layer and the second metal layer."

Neither Grzyb et al. nor Appel, whether alone or in combination, teach or suggest "wherein forming the inter-digitated capacitance structure further comprises forming a plurality of de-coupling capacitances between the inter-digitated capacitance structure, the first metal layer and the second metal layer." Grzyb et al. fails to teach or suggest that the capacitor 20 is an inter-digitated capacitance structure. Nowhere does Grzyb et al. disclose an inter-digitated capacitor structure.

The Office Action cites Column 8, lines 1-31 of Grzyb et al. and alleges

> Grzyb et al. disclose forming a plurality of de-coupling capacitances between the inter-digitated capacitance structure, the top metal layer and bottom metal layer." (Office Action, page 5).

However, this statement appears to be unsupported by the disclosure of Grzyb et al. Specifically, the capacitor 20 of Grzyb et al. does not provide "a plurality of de-coupling capacitances." Instead, the capacitor 20 provides a single capacitor having an oxide layer as a dielectric (Column 4, lines 1-5). Furthermore, the capacitor 20 is not an inter-digitated capacitance structure. Grzyb et al. thus fails to teach or suggest forming a plurality of de-coupling capacitances between the capacitor 20. In addition, the Office Action correctly notes that Appel fails to teach or suggest "a plurality of de-coupling capacitances" as claimed. (Office Action, page 6) For at least the foregoing reasons, Grzyb et al. in view of Appel fail to teach or suggest all the features of claims 4, 6-9, 11-13 and 15, and withdrawal of the rejection is respectfully requested.

Rejection of Claims 17-19 under 35 U.S.C. § 103(a)

The Office Action sets forth a rejection of claims 17-19 under 35 U.S.C. § 103(a) as allegedly being unpatentable over Appel in view of Grzyb et al. This rejection is respectfully traversed for at least the following reasons. Claim 17 has been cancelled and the features thereof have been incorporated into amended independent claim 16.

Amended independent claim 16 incorporates the features of cancelled claim 17. Independent claim 16 recites an integrated circuit comprising "a circuit function block having a predetermined circuit layout" and "an inter-digitated capacitance structure ... on top of the

circuit function block, wherein a plurality of dc-coupling capacitances are formed between the inter-digitated capacitance structure, a first metal layer, and a second metal layer."

Grzyb et al. fails to teach or suggest an inter-digitated capacitance structure. The capacitor 20 disclosed by Grzyb et al. is not an inter-digitated capacitance structure.

In addition, neither Appel nor Grzyb et al teach or suggest "a plurality of de-coupling capacitances" for at least the reasons set forth above. The Office Action cites Column 8, lines 1-31 of Grzyb et al. and alleges

> Grzyb et al. disclose de-coupling capacitances between the inter-digitated capacitance structure, the top metal layer and bottom metal layer. (Office Action, page 6).

However, this statement appears to be unsupported by the disclosure of Grzyb et al. Specifically, the capacitor 20 of Grzyb et al. does not provide "dc-coupling capacitances between the inter-digitated capacitance structure." Furthermore, the capacitor 20 is not an inter-digitated capacitance structure. In addition, the capacitor 20 is a single capacitor having an oxide layer as a dielectric (Column 8, lines 20-25). Grzyb et al. also fails to teach or suggest de-coupling capacitances between the capacitor 20 and top and bottom metal layers.

In addition, the Office Action correctly notes that Appel fails to teach or suggest "a plurality of de-coupling capacitances" as claimed. (Office Action, page 6) Appel discloses a MIM capacitor having five metal layers MET1-MET5 (Figure 2; Column 2, lines 30-35), but Appel fails to teach or suggest that the MIM capacitor provides a plurality of dc-coupling capacitances. Because claim 19 incorporate all the features of independent claim 16, Appel thus also fails to teach or suggest all the features of claim 19, at least by virtue of their dependency. For at least the foregoing reasons, Appel in view of Grzyb et al. fail to teach or suggest all the features of claim 19, and withdrawal of the rejection is respectfully requested.

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Rejection of Claims 5 and 14 under 35 U.S.C. § 103(a)

The Office Action sets forth a rejection of claims 5 and 14 under 35 U.S.C. § 103(a) as allegedly being unpatentable over Grzyb et al. in view of Appel, and further in view of Daubenspeck et al. This rejection is respectfully traversed for at least the following reasons.

Claim 5 incorporates all the features of independent claim 1, and claim 14 incorporates all the features of independent claim 11. For at least the reasons above, neither Grzyb et al. nor Appel teach or suggest the features recited in independent claims 1 and 16.

Daubenspeck et al. fails to remedy the deficiencies of Grzyb et al. and Appel.

Daubenspeck et al. discloses a capacitive circuit including a capacitor and a fuse link (Abstract). Daubenspeck et al. fails, however, to teach or suggest "forming a plurality of de-coupling capacitances between the inter-digitated capacitance structure, the first metal layer and the second metal layer" as recited in independent claim 11. Instead, the capacitive circuit disclosed by Daubenspeck et al. provides a single capacitance (Column 1, lines 55-65). In addition, Daubenspeck et al. fails to teach or suggest that the capacitor is formed "in an area above the circuit function block" as recited in claim 1. Instead, the capacitor shown in Figure 14 of Daubenspeck et al. is shown in isolation, without any reference to a circuit function block. For at least these reasons, Daubenspeck et al. fails to remedy the deficiencies of Grzyb et al. and Appel.

Newly Added Claims

Claims 21-23 have been added. Claim 21 depends from allowable claim 1 and is also allowable at least by virtue of its dependency. Claim 22 depends from allowable claim 11 and is also allowable at least by virtue of its dependency. Claim 23 depends from

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allowable claim 16 and is also allowable at least by virtue of its dependency. Claims 21-23 each recite "wherein the inter-digitated capacitance structure is formed above a cache memory", which is not taught or suggested by the prior art. Therefore, the Examiner is respectfully requested to allow claims 21-23.

Conclusion

In light of the foregoing, withdrawal of the rejections of record and allowance of this application are earnestly solicited. Should the Examiner believe that a telephone conference with the undersigned would assist in resolving any issues pertaining to the allowability of the above-identified application, please contact the undersigned at the telephone number listed below. Please grant any required extensions of time and charge any fees due in connection with this request to deposit account no. 08-2025.

Respectfully submitted,

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Dated: June 15, 2005

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